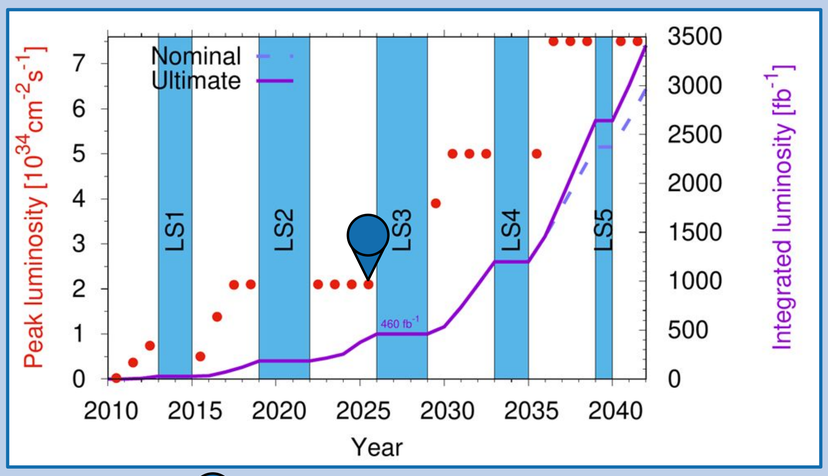
# Development of the new ATLAS TDAQ Dataflow system for the LHC High Luminosity Upgrade

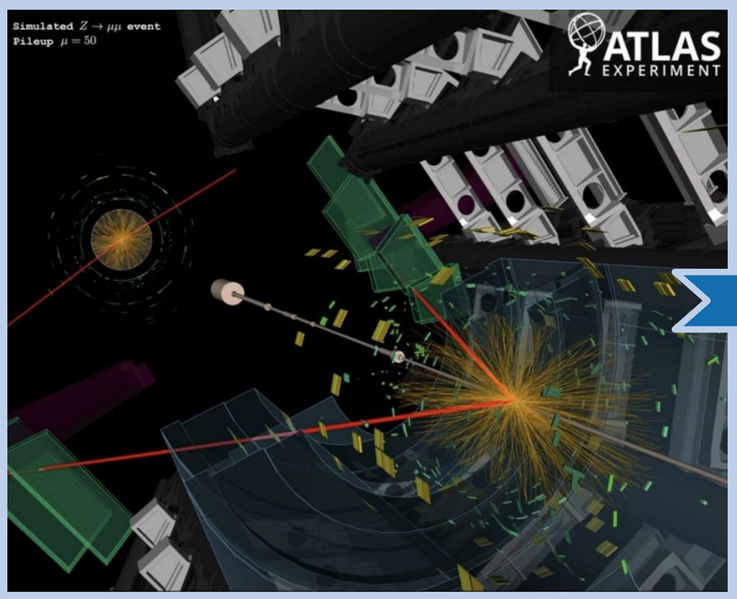
## The High Luminosity LHC upgrade

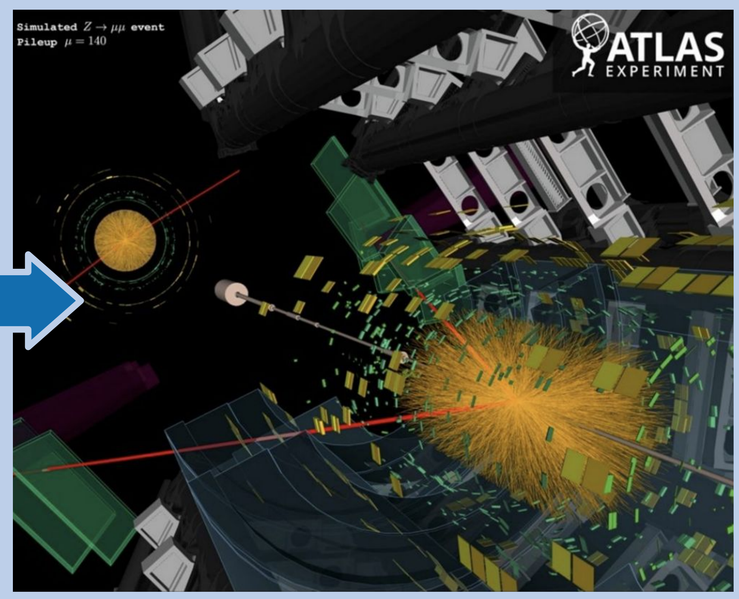
The LHC will do a major upgrade in the coming years to prepare for the following runs. Tha aim of this upgrade will be:

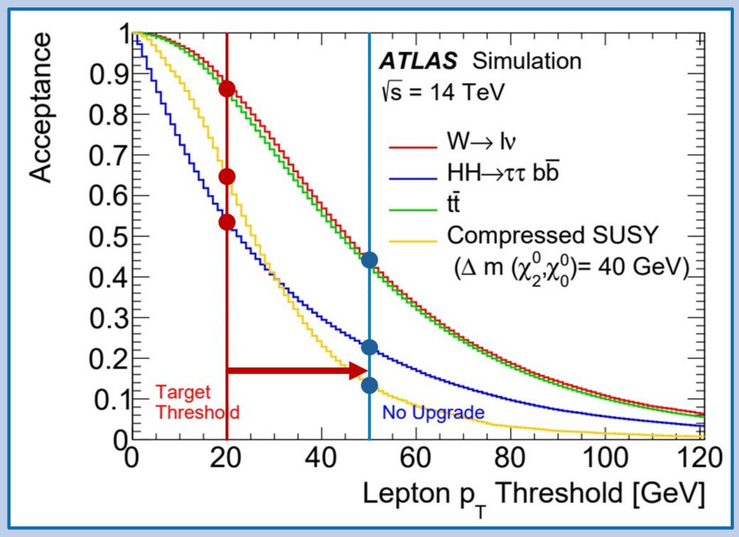
- Switch from discovery to **precision measurement**
- **Extend** the accelerator **lifetime** collecting as much data as possible
- Significantly **improve precision** for the Higgs sector
- Observe **very rare** new phenomena

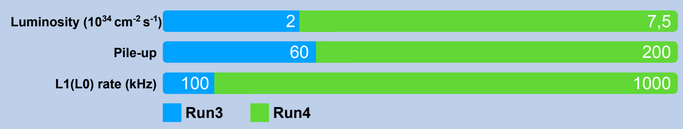



## THE DETECTOR DILEMMA



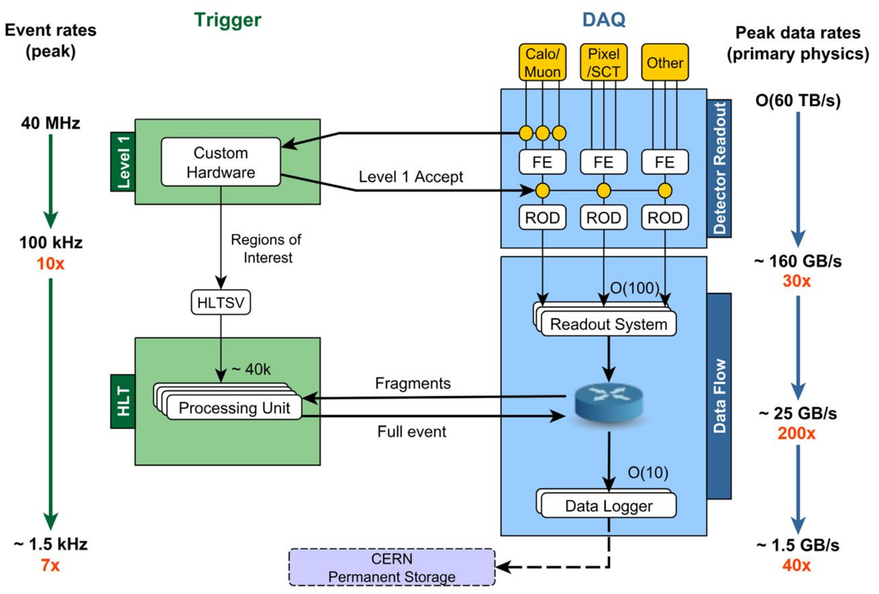

## A very challenging upgrade

Increasing the luminosity will also raise **Pile-up** from the current 60 **up to 200.** A higher pile-up translates to **higher background,** increasing the **difficulty** of particles tracking and reconstruction.

With the current detector, the increased background would severely impact data taking due to **hardware and DAQ limitation**. In this scenario, we would need to increase signal **thresholds** to be able to filter out the background, at the cost of **reducing signal acceptance** significantly.

To address the issue, the detector and the TDAQ system will undergo a **major upgrade**, **increasing** the trigger rate to **1 MHz**. This will let us keep the **target thresholds** improving efficiency.

## TRIGGER AND DAQ UPGRADE




The Trigger and Data Acquisition **system upgrade** will require handling a **10x** increase in input event **rate** and up to **30x** increase in total **data throughput**. This will heavily affect the **Dataflow** subsystem, the backbone used to transfer data from the detector readout to the Event Filter farm.

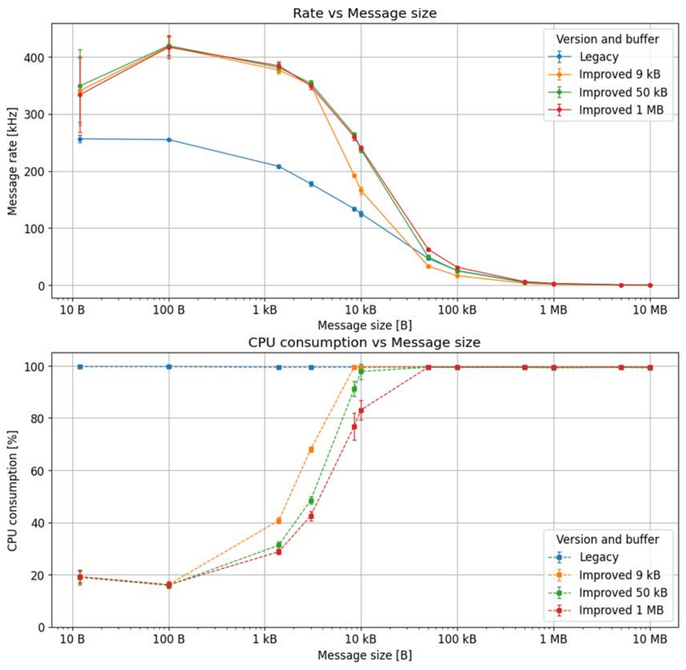
To keep the **filtering capabilities** in spite of the higher background, the new Event Filter will have to **collect all event fragments** before it can start processing. This requirements means a data throughput increase of **200 times!**

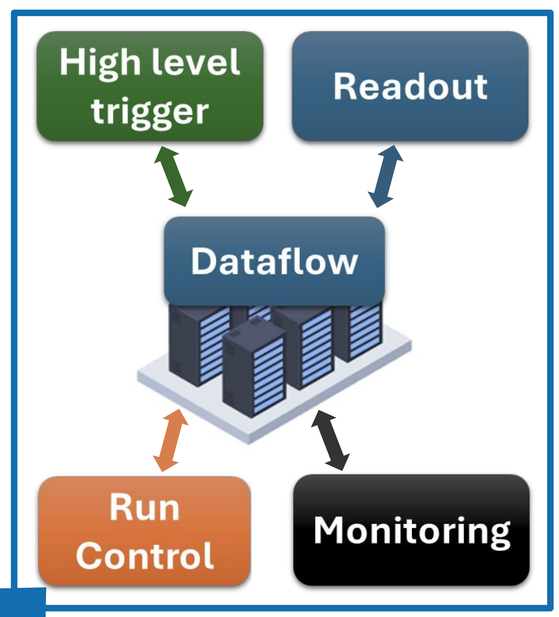
## LOOKING FOR SOLUTIONS

### System optimization

The current Dataflow system uses asynchronous programming techniques to manage data transfers and optimize resource usage (**ASIO**). The current solution, called **asyncmsg**, was **developed ad-hoc** by the Pavia group to handle the technical challenges of the previous runs and is being used since then.

Our research is focused on system **performance validation** on updated hardware. **Optimization** of the current solution is the **baseline of the upgrade**, and currently has improved its capabilities up to **2x data rate**, while also reducing CPU consumption **up to 80%**. Recent measurements show that this solution can **meet the requirements**, while providing **seamless integration** with the other DAQ components.




### Researching cutting edge technology

While improving the current system is our main goal, we are also exploring new cutting edge technologies used in the most demanding areas of the field. These includes high end options like **Remote Direct Memory Access**, promising significant resource usage reductions, while delivering very high performances.

The research on these technologies is essential to evaluate their applicability at the experiment scale and adapt to our use case.

ASYNCMSG boost C++ LIBRARIES

RDMA Remote Direct Memory Access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